

Professional Experience

QLogic / PathScale – CTO InfiniBand Products 2003 - Present

Joined PathScale in 2003 as a Distinguished Architect. PathScale was acquired by QLogic in 2006. Responsible for InfiniBand technical product strategy. Represent the company on the boards of the InfiniBand Trade Association and the OpenFabrics Alliance. Speaker at SC, ISC and SNW. Submitted three patent applications.

Adjunct Professor – San Francisco State University, Computer Science Department Summer 2003

Taught upper division computer science and software development courses. Topics include object-oriented design, compiler writing, large project software methodologies, byte-code virtual machine interpreters, and architectural implications of software structure and design. C++ and Java are used in these courses.

Visiting Professor – Northwestern University, Department of Electrical and Computer Engineering Winter 2002/3

Taught upper division computer architecture course and senior computer engineering design seminar. Topics included architectural interfaces, data path design, control structures, cache and storage hierarchies, buses and i/o systems. Course projects included design of an extensive ARM subset (with cache), MIPS-lite subset, and SoC designs using ASIC libraries and VHDL.

Consultant 2002–2003

Consulting projects include:

- Storage system strategy and product plan
- Technology due diligence of startup companies
- Patent expert research

Phototablet / Fotiva – Consultant 2001-2002

Developed architecture for innovative client based consumer software product, and server-network design (Weblogic and Tomcat). Acquired by Adobe.

Bpath – Vice President R&D 2000-2001

Responsible for R&D, including product development, partner technical integration, and website operations. Web services products included self-service customer tools and customer support systems. Website and internet services averaged 100K transactions per hour. Supported internet integration efforts with financial institutions and media properties. IT support for company-wide desktop and server systems. R&D teams in US and Israel.

Amdahl Corporation – SmartCard Group – Vice President, Operations 1998-2000

Directed operations for a division in the emerging smart card payments market. Global responsibilities with installed systems in North America, Europe, Middle East, Asia and Australia.

Amdahl Corporation – Corporate Technology Group – Chief of Staff 1992-1998

Developed transition plan to place mainframe product line on emerging CMOS technology curve. Negotiated processor joint development agreement with Fujitsu to align R&D model with compressed product margins. Worked to restructure other product groups by redirecting Storage business and product plans as well as forming two new business units to move company into higher growth markets. Responsible executive for IT infrastructure, supporting 1,200 engineers.

Amdahl Corporation – Products Group – Senior Director, Architecture and Planning

1981-1992

Headed Architecture and Product Planning groups. Responsible for product compatibility, internal architecture design and specification, product requirements, product planning, competitive analysis and trusted systems design. Innovative internal product architecture designs for server virtualization and consolidation based on virtual machine architectures, advanced operating systems process management, high performance task switching and ease of operations. Established architecture management process and chaired Architecture Review Board. Responsible for architecture design and technical coordination with strategic partners. R&D teams in US and Japan.

University of California, Berkeley – Computer Science Division - Visiting Professor

1980-1981

Taught upper division computer architecture sequence during the Risc-revolution era. Supervised research on high-performance Risc processor designs and instruction set specification.

Digital Equipment Corporation – Product Development and Research Group

1974-1980

Developed high-end servers and headed Computer Systems Architecture research. Research initiatives included string processing instruction set enhancements, secure computing, reliable computing structures and multiprocessor structures. Projects in multiprocessor structures and reliable computing were conducted with Carnegie-Mellon University (CMU).

Managed engineering projects for secure operating system design (VMS/SE) and PDP-11/VAX-11 architecture design. Supervised university research partnerships on multi-processor structures for high-performance (Cm*) and high-reliability (triplicated LSI-11).

RCA – Advanced Technology Laboratory and Aerospace Systems Division – Senior Engineer

1970-1974

At RCA, architected and designed VLSI chips for large-scale pattern matching application – customer was Naval Research Lab's Associative Processor Microprocessor Element program. Completed chip architecture, design. Chip fabricated and provided to customer.

Designed and implemented real-time operating systems and compilers for automated testing applications. OS was part of demonstration project for Army Tank and Automotive Command – instrumented Jeep was successfully diagnosed for numerous engine maintenance problems. Demonstration was successful and resulted in expansion of the project to include other military vehicles. Atlas language compiler and associated Java-like byte-code virtual machine execution environment was developed for Navy S3-A aircraft maintenance program.

Classified work on aircraft missile warning system.

Additional Activities

IEEE Computer Society Technical Committee on Computer Architecture. Past officer of ACM SigArch. Life-member member of Tau Beta Pi and Eta Kappa Nu. Member of IEEE and Senior Member of ACM.

Organized and General Chair for the original Architecture Symposium on Architectural Support for Program Languages and Operating Systems (ASPLOS I).

Taught graduate courses in programming languages, data structures and systems programming at Northeastern University and University of Lowell.

Holder of 2 US Patents.

Education

Lehigh University – BSEE 1970 / MSEE 1971 - Master's thesis on VLSI systems design. Design of VLSI associative processor element. Graduate research project on high-performance pattern matching and recognition.

Harvard University - Graduate course work in computer science. Design studies of virtual machine architectures.